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a gate electrode provided adjacent to said channel region with a gate insulating film therebetween;

a first gate interconnection formed on said insulating surface;

a first layer comprising metal provided on said insulating surface and being in direct contact with said first gate interconnection and being connected with one of said source region and said drain region;

a second layer comprising metal provided on said insulating surface and being in direct contact with the other one of said source region and said second region;

an interlayer dielectric provided over said gate electrode, said first layer comprising metal and said second layer comprising metal;

a first contact hole provided over said first layer comprising metal in said interlayer dielectric;

a second contact hole provided over said second layer comprising metal in said interlayer dielectric;

a second interconnection comprising aluminum provided over said interlayer dielectric and connected with said first layer comprising metal through said first contact hole; and

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(concluded)
a third interconnection comprising aluminum provided over said interlayer dielectric and connected with said second layer comprising metal through said second contact hole,

wherein said first and second contact holes are located outside said source region, said drain region and said first gate interconnection.

73. (Amended) A semiconductor device comprising:

a semiconductor island comprising silicon provided on an insulating surface;

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a source region and a drain region provided in said semiconductor island;

a channel region provided in said semiconductor island between said source region and said drain region;

a gate electrode provided adjacent to said channel region with a gate insulating film therebetween;

a first gate interconnection formed on said insulating surface;

a first layer comprising metal provided on said insulating surface and being in direct contact with said first gate interconnection and being connected with one of said source region and said drain region, said first layer comprising metal

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being connected with said first gate interconnection through no contact hole;

a second layer comprising metal provided on said insulating surface and being in direct contact with the other one of said source region and said second region;

an interlayer dielectric provided over said gate electrode, said first layer comprising metal and said second layer comprising metal;

a first contact hole provided over said first layer comprising metal in said interlayer dielectric;

a second contact hole provided over said second layer comprising metal in said interlayer dielectric;

a second interconnection comprising aluminum provided over said interlayer dielectric and connected with said first layer comprising metal through said first contact hole; and

a third interconnection comprising aluminum provided over said interlayer dielectric and connected with said second layer comprising metal through said second contact hole,

wherein said first and second contact holes are located outside said source region, said drain region and said first gate interconnection.

74. (Amended) A semiconductor device comprising:

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a semiconductor island comprising silicon provided on an insulating surface;

a source region and a drain region provided in said semiconductor island;

a channel region provided in said semiconductor island between said source region and said drain region;

a gate electrode provided adjacent to said channel region with a gate insulating film therebetween;

a first gate interconnection formed on said insulating surface;

a first layer comprising metal provided on said insulating surface and being in direct contact with said first gate interconnection and being connected with one of said source region and said drain region;

a second layer comprising metal provided on said insulating surface and being in direct contact with the other one of said source region and said second region;

an interlayer dielectric comprising silicon nitride provided over said gate electrode, said first layer comprising metal and said second layer comprising metal;

a first contact hole provided over said first layer comprising metal in said interlayer dielectric;

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a second contact hole provided over said second layer comprising metal in said interlayer dielectric;

a second interconnection comprising aluminum provided over said interlayer dielectric and connected with said first layer comprising metal through said first contact hole; and

a third interconnection comprising aluminum provided over said interlayer dielectric and connected with said second layer comprising metal through said second contact hole,

wherein said first and second contact holes are located outside said source region, said drain region and said first gate interconnection.

75. (Amended) A semiconductor device comprising:

a substrate having an insulating surface;

a semiconductor island comprising silicon provided over said insulating surface;

a source region and a drain region provided in said semiconductor island;

a channel region provided in said semiconductor island between said source region and said drain region;

a gate electrode provided adjacent to said channel region with a gate insulating film therebetween;

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a first gate interconnection formed on said insulating surface;

a first layer comprising metal provided on said insulating surface and being in direct contact with said first gate interconnection and being connected with one of said source region and said drain region;

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(continued)
a second layer comprising metal provided on said insulating surface and being in direct contact with the other one of said source region and said second region;

an interlayer dielectric comprising silicon oxide provided over said gate electrode, said first layer comprising metal and said second layer comprising metal;

a first contact hole provided over said first layer comprising metal in said interlayer dielectric;

a second contact hole provided over said second layer comprising metal in said interlayer dielectric;

a second interconnection comprising aluminum provided over said interlayer dielectric and connected with said first layer comprising metal through said first contact hole; and

a third interconnection comprising aluminum provided over said interlayer dielectric and connected with said second layer comprising metal through said second contact hole,

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wherein said first and second contact holes are located outside said source region, said drain region and said first gate interconnection.

76. (Amended) A semiconductor device comprising:

a substrate having an insulating surface;

a semiconductor island comprising silicon provided over said insulating surface;

a source region and a drain region provided in said semiconductor island;

a channel region provided in said semiconductor island between said source region and said drain region;

a gate electrode comprising a doped polycrystalline silicon provided adjacent to said channel region with a gate insulating film therebetween;

a first gate interconnection formed on said insulating surface;

a first layer comprising metal provided on said insulating surface and being in direct contact with said first gate interconnection and being connected with one of said source region and said drain region;

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a second layer comprising metal provided on said insulating surface and being in direct contact with the other one of said source region and said second region;

an interlayer dielectric provided over said gate electrode, said first layer comprising metal and said second layer comprising metal;

a first contact hole provided over said first layer comprising metal in said interlayer dielectric;

a second contact hole provided over said second layer comprising metal in said interlayer dielectric;

a second interconnection comprising aluminum provided over said interlayer dielectric and connected with said first layer comprising metal through said first contact hole; and

a third interconnection comprising aluminum provided over said interlayer dielectric and connected with said second layer comprising metal through said second contact hole,

wherein said first and second contact holes are located outside said source region, said drain region and said first gate interconnection.

83. (Amended) The device of claim 75 wherein said first layer comprising metal is connected with said first gate interconnection through no contact hole.

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85. (Amended) The device of claim 76 wherein said first layer comprising metal is connected with said first gate interconnection through no contact hole.

86. (Amended) A display device comprising:
a substrate having an insulating surface;
a semiconductor island comprising silicon provided over said insulating surface;
a source region and a drain region provided in said semiconductor island, said source region and said drain region comprising a silicide of a metal;
a channel region provided in said semiconductor island between said source region and said drain region;
a gate electrode provided adjacent to said channel region with a gate insulating film therebetween;
a first gate interconnection formed on said insulating surface;
a first layer comprising said metal provided on said insulating surface and being in direct contact with said first gate interconnection and being connected with one of said source region and said drain region;

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a second layer comprising metal provided on said insulating surface and being in direct contact with the other one of said source region and said second region;

an interlayer dielectric provided over said gate electrode, said first layer comprising said metal and said second layer comprising metal;

a first contact hole provided over said first layer comprising said metal in said interlayer dielectric;

a second contact hole provided over said second layer comprising metal in said interlayer dielectric;

a second interconnection comprising aluminum provided over said interlayer dielectric and connected with said first layer comprising said metal through said first contact hole; and

a third interconnection comprising aluminum provided over said interlayer dielectric and connected with said second layer comprising metal through said second contact hole,

wherein said first and second contact holes are located outside said source region, said drain region and said first gate interconnection.

87. (Amended) A semiconductor device comprising:

a semiconductor island comprising silicon provided on an insulating surface;

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a source region and a drain region provided in said semiconductor island, said source region and said drain region comprising a silicide of a metal;

a channel region provided in said semiconductor island between said source region and said drain region;

a gate electrode provided adjacent to said channel region with a gate insulating film therebetween;

a first gate interconnection formed on said insulating surface;

a first layer comprising said metal provided on said insulating surface and being in direct contact with said first interconnection and being connected with one of said source region and said drain region, said layer comprising said metal being connected with said gate interconnection through no contact hole;

a second layer comprising metal provided on said insulating surface and being in direct contact with the other one of said source region and said second region;

an interlayer dielectric provided over said gate electrode, said first layer comprising said metal and said second layer comprising metal;

a first contact hole provided over said first layer comprising said metal in said interlayer dielectric; and

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a second contact hole provided over said second layer comprising metal in said interlayer dielectric;

a second interconnection comprising aluminum provided over said interlayer dielectric and connected with said first layer comprising said metal through said first contact hole; and

a third interconnection comprising aluminum provided over said interlayer dielectric and connected with said second layer comprising metal through said second contact hole,

wherein said first and second contact holes are located outside said source region, said drain region and said first gate interconnection.

95. (Amended) A display device according to claim 61, wherein said first gate interconnection is provided in a same layer as said gate electrode.

96. (Amended) A semiconductor device according to claim 73, wherein said first gate interconnection is provided in a same layer as said gate electrode.

97. (Amended) A semiconductor device according to claim 74, wherein said first gate interconnection is provided in a same layer as said gate electrode.

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98. (Amended) A semiconductor device according to claim 75, wherein said first gate interconnection is provided in a same layer as said gate electrode.

99. (Amended) A semiconductor device according to claim 76, wherein said first gate interconnection is provided in a same layer as said gate electrode.

100. (Amended) A display device according to claim 86, wherein said first gate interconnection is provided in a same layer as said gate electrode.

101. (Amended) A semiconductor device according to claim 87, wherein said first gate interconnection is provided in a same layer as said gate electrode.
